UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,410	11/13/2001	Whu-Ming Young	0200109C1	7155

25700 7590 07/19/2004

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
FAN, CHIEH M	

ART UNIT	PAPER NUMBER
2634	16

DATE MAILED: 07/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,410	YOUNG ET AL.	
	Examiner	Art Unit	
	Chieh M Fan	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,32-36,61-72,75-79,81-84,86,88,92,93,95-105,113 and 115-120* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-16,32-36,61-71,75-77,79,81-84,86,88,92,93,95-99,101-105,113,117,118 and 120* is/are allowed.

6)☒ Claim(s) *78,100,115,116 and 119* is/are rejected.

7)☒ Claim(s) *72* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 72 is objected to because of the following informalities: "(d) generating" in line 2 should be changed to --- (e) generating ---. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 78 and 100 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 78 recites the limitation "said host signal processing circuitry" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. It appears that claim 78 should depend on claim 77.

Claim 100 recites the limitation "said clock rate" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 115 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Ramachandran (U.S. Patent No. 6,493,326) and Anderson et al. (U.S. Patent No. 5,532,556, "Anderson" hereinafter).

The admitted prior art associated with Figs. 1A and1B of the present application teaches a method of communicating data over a data link (120 in Fig. 1A) connecting a first integrated circuit (130 in Figs. 1A and 1B) located on a first circuit board (131 in Fig. 1B) and a second integrated circuit (110 in Figs. 1A and 1B) located on the a second circuit board (111 in Fig. 1B), the method comprising the steps of:

(a) communicating first transmit data from the first integrated circuit to the second integrated circuit over the data link using a first transmission channel (SDATA-OUT in Fig. 1A); and

(b) communicating first receive data from the second integrated circuit to the first integrated circuit over the data link using a first receive channel (SDATA-IN in Fig. 1A), said first receive channel and said first transmission channel being separate; and

(c) clocking data transmissions in said first transmission channel and/or said first receive channel over the data link using a clock signal (BITCLK in Fig. 1A).

Further note that since the transmission channel and the receive channel are clocked by the same bit clock signal, the transmission clock rate and the receive clock rate are equal. That is, the transmission clock rate and the receive rate have a ratio of one, which is an integer.

The admitted prior art does not teach the cock signal is a scaleable clock signal, wherein said scaleable clock signal is adjusted for the data link between the first integrated circuit and the second integrated circuit so that the data link uses a scaleable clock rate to support a data transfer rate required for said first transmission channel and/or said first receive channel.

Ramachandran teaches a variable rate vocoder that transmits the audio data at a lower rate to a modem when there is low speech activity (col. 4, lines 2-4). Anderson teaches a protocol for transferring audio data between two audio functional units at multiple rates (see abstract). To support the protocol, an incoming 24.576 MHz clock is divided by 4, 3, or 2 to produce sample bit rates for 24, 32, or 48 KHz, respectively. This bit clock is used for generating serial port clock rates of 6.144, 8.192, or 12.288 MHz.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the clock signal of the admitted prior art with a scaleable clock signal to support a multiple-rate transferring protocol, and thereby to improve the flexibility.

6. Claims 115 and 119 are rejected under 35 U.S.C. 103(a) as being unpatentable over Timm et al. (U.S. Patent No. 6,055,268) in view of the admitted prior art.

Regarding claim **115**, Timm teaches a method of communicating data over a data link (120 in Fig. 1A) connecting an analog codec (170, 172 in Fig. 1b) and a digital controller (160, 150 in Fig. 1b), the method comprising the steps of:

(a) communicating first transmit data from the digital controller to the analog codec over the data link using a first transmission channel (150 to 170 in Fig. 1b); and

(b) communicating first receive data from the analog codec to the digital controller over the data link using a first receive channel (172 to 150 in Fig. 1b), said first receive channel and said first transmission channel being separate; and

(c) clocking data transmissions in said first transmission channel and/or said first receive channel over the data link using a scaleable clock signal (SAMPLE CLOCK, DIV in Fig. 1b);

wherein the clock signal is variable to accommodate a plurality of different xDSL transmission protocols (col. 6, lines 54-55); and

wherein the transmission clock rate and the receive clock rate are related by an integer ratio (see DAC SAMPLE CLOCK, ADC SAMPLE CLOCK and DIV in Fig. 1b).

Timm does not teach the digital controller is located on the motherboard (i.e., the claimed "first circuit board") of a PC and the analog codec is located on a separate board (i.e., the claimed "second circuit board"). However, the admitted prior art described in the background section and in Fig. 1 teaches separating the analog and

digital portions of a high-speed modem. The digital controller is placed on the motherboard and the analog codec is placed on a card that is physically separated from the motherboard. Such arrangement would keep the analog codec free from the electronic noise from the electronic components on the motherboard. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the digital controller on the motherboard and place the analog codec on a card that is physically separated from the motherboard, so as to keep the analog codec free from the electronic noise from the electronic components on the motherboard.

Regarding claim **119**, Timm teaches a method of communicating data over a data link (120 in Fig. 1A) connecting an analog codec (170, 172 in Fig. 1b) and a digital controller (160, 150 in Fig. 1b), the method comprising the steps of:

(a) communicating first transmit data from the digital controller to the analog codec over the data link using a first transmission channel (150 to 170 in Fig. 1b); and

(b) communicating first receive data from the analog codec to the digital controller over the data link using a first receive channel (172 to 150 in Fig. 1b), said first receive channel and said first transmission channel being separate;

(c) clocking data transmissions in said first transmission channel and/or said first receive channel over the data link using a scaleable clock signal (SAMPLE CLOCK, DIV in Fig. 1b); and

(d) providing a data word clock (SYMBOL CLOCK in Fig. 1b) for effectuating said data transmission in the form of data words over the data link, said data words including

a fixed number of data bits such that the data word clock has a period corresponding to multiple clock signals; and

wherein the clock signal is variable to accommodate a plurality of different xDSL transmission protocols (col. 6, lines 54-55).

Timm does not teach the digital controller is located on the motherboard (i.e., the claimed "first circuit board") of a PC and the analog codec is located on a separate board (i.e., the claimed "second circuit board"). However, the admitted prior art described in the background section and in Fig. 1 teaches separating the analog and digital portions of a high-speed modem. The digital controller is placed on the motherboard and the analog codec is placed on a card that is physically separated from the motherboard. Such arrangement would keep the analog codec free from the electronic noise from the electronic components on the motherboard. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the digital controller on the motherboard and place the analog codec on a card that is physically separated from the motherboard, so as to keep the analog codec free from the electronic noise from the electronic components on the motherboard.

7. Claim 116 is rejected under 35 U.S.C. 103(a) as being unpatentable over Timm et al. (U.S. Patent No. 6,055,268) in view of the admitted prior art as applied to claim 115 above, and further in view of Gulick et al. (U.S. Patent No. 5,404,459).

Timm in view of the admitted prior art teaches the claimed invention except a control register for providing the integer ratio.

However, it is common in the art to program a data rate in a control register so as to provide flexibility of a communication system. Gulick teaches programming the data rate in a control register (col. 7, lines 31-32). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide a control register to control the data rate of the DSL modem of Timm so as to provide flexibility of the system of Timm/admitted prior art.

Allowable Subject Matter

8. Claims 1-16, 32-36, 61-71, 75-77, 79, 81-84, 86, 88, 92, 93, 95-99, 101-105, 113, 117, 118 and 120 are allowed. Claim 72 would be allowable if rewritten to overcome the claim objection above. Claims 78 and 100 would be allowable if rewritten to overcome the rejection under 35 USC 112, second paragraph above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (703) 305-0198. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703) 305-4714. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Chieh M Fan
Primary Examiner
Art Unit 2634

cmf
July 10, 2004